

Top-down analysis critical for power-aware design success

Preeti Gupta

Technical Marketing Manager
Sequence Design

In addition to performance and area, power has emerged as a key consideration in the semiconductor industry. Power has transformed from a mere number to a critical factor that needs to be managed at every step of the design flow. Indeed, for many wireless and handheld applications, power can make or break a product in the market.

Concurrently, several trends mandate a "power-aware" design methodology, to reduce power consumption as well as to manage the corrosive effects of mishandled power on the rest of the design.

- Shrinking geometries allow more components to be packed into smaller areas that result in higher power density and, consequently, temperature variations. The components of power leakage that were insignificant in larger processes need to be considered now.
- With cell phone, laptop and other portable electronics companies competing on extended battery life, it's necessary to minimise standby power along with active power.
- Yield has also emerged as a key concern; power, and its consequences contribute to the uncertainty.

Early analysis is key

Designers manage power at differing levels of abstraction depending on their power needs. The thumb rule is: "The earlier you design for power, the larger your savings." A top-down approach is unavoidable since nearly 80 per cent of a chip's total power budget is determined by decisions made at or before RTL. Innovative

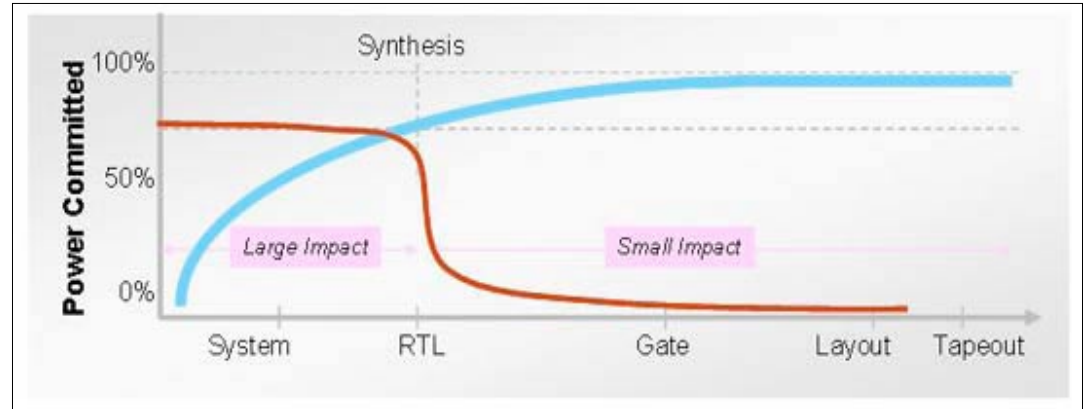


Figure 1: Early attention to power necessary for maximum power savings.

designers spend significant time at the system and RT level designing for power. Exploring different architectures for power must be done early in the design flow; as it is too costly and time-consuming during implementation.

Though the opportunity to save power reduces as one proceeds down levels of abstraction, predicting power accuracy is the challenge at higher levels. Tools and methodologies at RTL should predict the behaviour of downstream tools and silicon to achieve accuracy. This can be done by well characterised power models in the vendor library. The RTL power analysis tool must also be comprehensive in modelling all components of SoCs while translating RTL code-clock trees, high fan-out signal nets, datapath, control logic in addition to macros like I/Os, memories as well as hard IP. With the right tools and methodology, designers can predict power at RTL within 20 per cent, or even better, when compared with gate-level power.

RTL power analysis

Majority of companies that worry about power have tools and methodology for power analysis at RTL. Some companies that use system level tools to select architectures based on perfor-

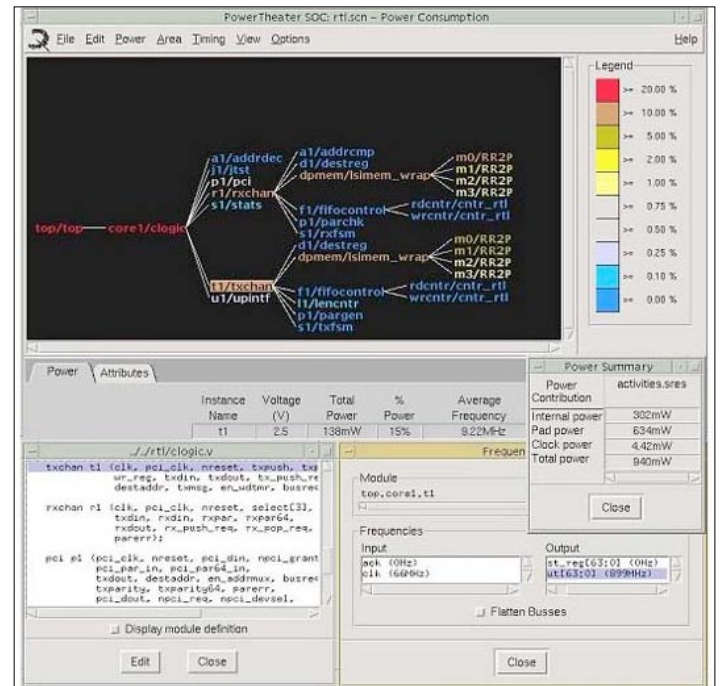


Figure 2: RTL power analysis provides power-per-function visibility.

mance vs. area trade-offs are also plugging in power analysis as the third metric.

RTL power analysis has number of advantages over gate level. There are some obvious advantages in terms of sheer capacity and performance throughput which are both >10x compared to gates. Yet another benefit is in generation of input simulation data that is at least an order (or two) of magnitude faster at RTL than at gate level.

One of the values at RTL that is obscure is the few minutes

it takes to juggle power trade-offs. Power savings achieved in a few hours by complex power management techniques can be analysed without making any effort in actual implementation. Another benefit of power analysis at RTL is association of power with a function that can be traced back to a source line of RTL code. Contrast that with hundreds of gates that make up the multiplier in a gate netlist vs. a single line of RTL source code. This seemingly small feature opens up a new way of under-

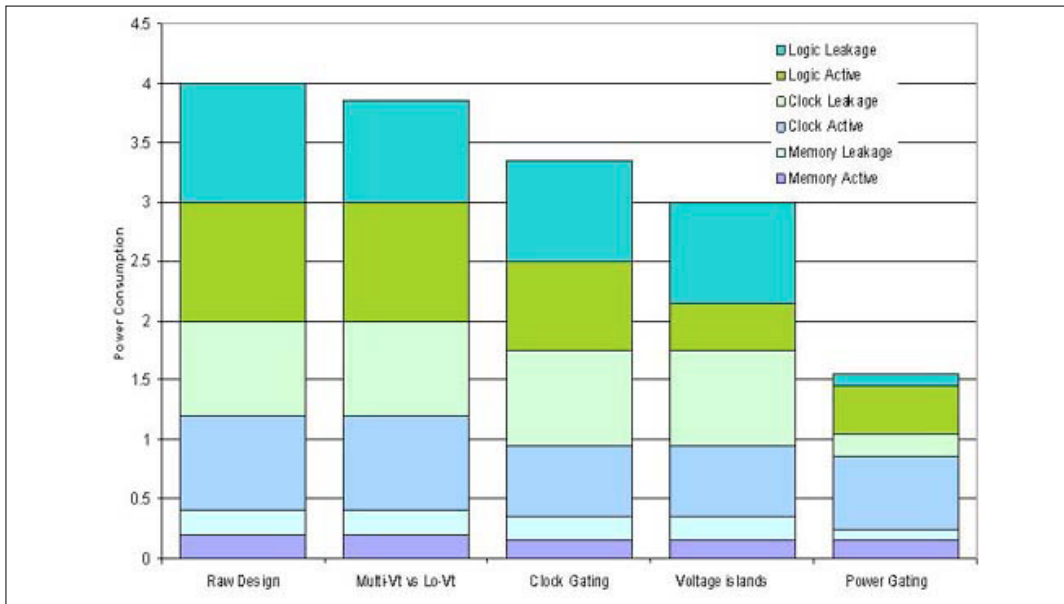


Figure 3: RTL analysis of power reduction with different power reduction techniques using Sequence Design's PowerTheater.

standing where and how power is consumed.

Effective power reduction

Several emerging power reduction techniques are in use today. The world of low-power design, however, is not simple since it has to work within the additional constraints of timing and area. Designers require understanding of performance and area trade-offs with different power saving techniques. Additionally, analysis of power savings, which can be achieved with one or more techniques, is needed before a great deal of time, effort and expense is invested in implementation.

The following graph demonstrates the benefits of early analysis with results on a sample handheld design. The RTL did not have any special code for any power reduction technique. The power was measured to be around 4W with a target specification of 2W. Power savings were explored at RTL for four common power reduction techniques using Sequence Design's PowerTheater. Without changing the RTL code, the tool analysed the impact of power savings by clock gating, mixed threshold voltage, voltage islands and power gating. These techniques are known to provide significant power savings when used in the correct manner. The techniques were turned on in a cumulative manner while the analysis of power savings

with clock gating was performed on top of savings with mixed threshold. Using this analysis, the designers were able to determine the set of techniques required to meet their power goal.

Activity crucial to power-related decisions

Activity is routinely used in tools and methodologies for power analysis. However, very few designers pay attention to design activity in its critical role for power reduction. Any methodology that considers power reduction independent of activity is incomplete and inefficient. Consider an

instance where a clock is gated with an enabled signal that is always on. Another example is a sleep signal for power gating that turns off power to a block for a very short duration of time.

Analysing and understanding design activity empowers the designer to not only use power saving techniques effectively but also eliminate power bugs. One such example is residual activity, and thereby wasted power, while the logic is idle. Or consider an IP from a previous generation chip, where power was not critical, that can now be optimised for low power.

The final word

Success in power management requires a "power-aware" mindset, in which power is analysed often as well as early throughout the design cycle. This top-down approach is exemplified by RTL power analysis, providing an early and accurate picture of power that achieves greatest savings.

At the system level, multiple EDA firms are enabling ESL performance and area exploration in C++, SystemC and SystemVerilog, but Sequence is the *defacto* standard for high-level power estimation for ESL flows. Sequence RTL power estimation technology integrates with ESL synthesis and simulation environments to provide power exploration for SoC platforms. This flow allows designers to take advantage of productivity gains; to optimise early for power in addition to performance and area, and to explore a variety of architectures rapidly.

As power issues become even more crucial at 65nm and below, it becomes increasingly important to estimate power early, and often! At RTL, and even above RTL, power reduction can have the significant effect on chip and package costs, battery life and market share of electronic products.

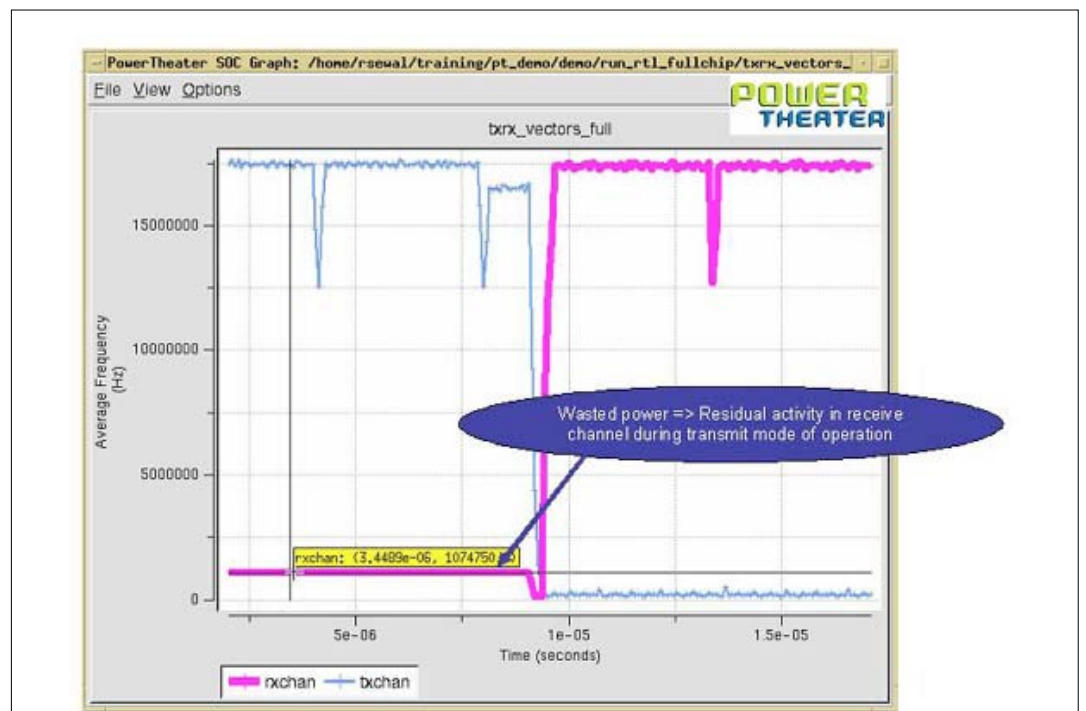


Figure 4: Activity over time waveforms using Sequence Design's PowerTheater.